WHAT IS CLAIMED IS:

1. An access circuit for receiving address data from a control circuit and transferring digital data to and from a buffer memory in a plurality of access data units, the access circuit comprising:

a decoder for decoding the address data, wherein the decoder generates a data unit designation signal for designating one of the access data units in accordance with the address data; and

an interface for accessing the buffer memory from a head address designated by the address data in the access data unit designated by the data unit designation signal.

2. The access circuit according to claim 1, further comprising:

a request generator for generating a plurality of request signals, each corresponding to a respective one of the access data units, wherein the request generator provides the interface with one of the request signals in accordance with the access data unit designated by the data unit designation signal, and the interface accessing the buffer memory in the access data unit corresponding to the one of the request signals.

3. The access circuit according to claim 2, wherein the data unit designation signal has a plurality of bits, the access circuit further comprising:

a latch section connected between the decoder and the request generator, wherein the latch section includes a plurality of latch circuits, each holding a respective one of the bits, and the request generator generating one of the request signals in accordance with the output of the latch

section.

4. The access circuit according to claim 1, wherein the plurality of access data units include one byte, one word, and two words.

5. An access circuit for receiving address data from a control circuit and transferring digital data to and from a buffer memory in a plurality of access data units, the access circuit comprising:

a decoder for decoding the address data, wherein the decoder generates a data unit designation signal having a plurality of bits to designate one of the access data units in accordance with the address data;

a latch section connected to the decoder and including a plurality of latch circuits, each for holding a respective one of the bits;

a request generator connected to the latch section to generate a request signal corresponding to one of the access data units in accordance with the output of the latch section; and

an interface connected to the request generator to access the buffer memory from a head address designated by the address data in the access data unit designated by the data unit designation signal.

6. An access circuit for use with an operation clock signal and receiving address data from a control circuit and transferring digital data to and from a buffer memory in a plurality of access data units, the access circuit comprising:

a decoder for decoding the address data, wherein the decoder generates a data unit designation signal for

designating one of the access data units in accordance with the address data; and

an interface for accessing the buffer memory from a head address designated by the address data in the access data unit designated by the data unit designation signal, wherein first data transfer lines are connected to the interface within the access circuit and second data transfer lines are connected between the interface and the buffer memory, and the number of the first data transfer lines is two times greater than the number of the second data transfer lines, and the frequency of a transfer clock signal used for transferring data between the interface and the buffer memory is two times greater than that of the operation clock signal; and

wherein the interface switches the number of times the digital data is accessed via the second data transfer lines during a single cycle of the operation clock signal.

7. The access circuit according to claim 6, wherein the interface changes the access data unit by changing the quantity of clock pulses of the transfer clock signal used for a single access.

8. An access circuit for receiving address data from a control circuit and arranged between the control circuit and a buffer memory, the access circuit comprising:

a decoder for decoding address data received from the control circuit;

a request generator for generating a request signal that designates one of a plurality of access data lengths in accordance with a decoding result of the decoder; and

an interface connected to the request generator to read data from the buffer memory in the access data length

designated by the request signal.

9. The access circuit according to claim 8, wherein the interface accesses the buffer memory in each of the access data lengths.

10. The access circuit according to claim 8, wherein the decoder generates a data unit designation signal indicating a decoding result of the address data.

11. The access circuit according to claim 10, wherein the request generator provides the interface with the request signal that is selected from a plurality of request signals in accordance with the data unit designation signal.

12. The access circuit according to claim 11, wherein the plurality of access data lengths include one byte, one word, and two words.